



STRATEGIC TEST

AN004 - Comparison of UF2 cards and UF cards

This application note gives you an overview on the changes from UF series to UF2 series. It will show all differences between the two card families for different aspects of the hardware. However, before relying on this application note please have a look at the latest manual version of the UF2 series to see the current details there.

This application note is for experienced users of the UF card series who wish to have some more information on the UF2 series and who want to see the fundamental differences that they have to expect when changing from one series to the other.

Hardware

All hardware details of the UF2 series are based on the first series version 1.x. All hardware details of the UF series are based on the version that was available when this application note was made. This is version 15.x (Hardware version 1.4).

Base card	UF2 card series	UF card series
Size of the base card	full size PCI length	full size PCI length
Interface	PCI-X interface capable of running with 33 MHz or 66 MHz PCI bus speed. Fits into any 32 or 64 bit PCI/PCI-X slot	PCI interface running with 33 MHz PCI bus speed. Fits into any 32 or 64 bit PCI/PCI-X slot
Maximum theoretical PCI bus transfer speed	264 MB/s	132 MB/s
Reached maximum transfer speed on 33 MHz PCI	115 MB/s	105 MB/s
Reached maximum transfer speed on 66 MHz PCI-X	230 MB/s	105 MB/s
Memory	UF2 card series	UF card series
Memory options	64 MB, 128 MB, 256 MB, 512 MB, 1 GB, 2GB, 4GB	16 MB, 32 MB, 64 MB, 128 MB, 256 MB, 512 MB
FIFO buffer usage	Uses the complete on-board memory as FIFO buffer	Uses the on-board memory for a double buffering. Used buffer size is programmed. One of the double buffers is transferred completely if it's full
Granularity of programmable memory size	Minimum 8 samples up to installed memory in steps of 4 samples independent of the number of activated 8 or 16 bit channels.	Minimum and stepsize depend on number of activated channels: 64 / channels / bytes per sample. Memsize can be up to the installed memory.
Granularity of programmable posttrigger	Up to 8 GSample in steps of 4 samples	Stepsize depends on number of activated channels: 64 / channels / bytes per sample. Maximum depends on the number of activated channels: 256 MSamples / channels / bytes per sample
Later memory update	Possible without extra charge	Possible but including an extra charge as parts are soldered to the PCB
Data ordering in memory	Depends on the number of activated modules only	Depends on the number of activated modules, the number of bytes per sample and the used mode (standard or FIFO)
FIFO mode sampling speed limitations	No limitations, all sampling rates, all modes available within FIFO mode	FIFO mode is limited to a maximum of 250 MB/s sum transfer from module(s) to on-board memory. This limit is even valid for Multiple Recording and Gated Sampling
DMA mode of data transfer	Busmaster Scatter-Gather DMA with hardware demand mode (more robust against system background jobs and other tasks)	Busmaster Scatter-Gather DMA handled by the kernel driver
Data transfer for timestamps (and ABA)	Second busmaster Scatter-Gather DMA engine with hardware demand mode	Kernel driver base PIO mode
Channel Selection	UF2 card series	UF card series
1 channel mode	Any channel on the card can be used (if not using interlace mode), even one channel located on module B	Only channel 0 can be activated
2 channel mode	Any two channels on the card can be used (if not using interlace), even two channels located on module B	Only channel 0 + channel 1 or channel 0 + first channel on module B can be activated
4 channel mode	Nearly any four channels on the card can be used as long as either all channels are on one module or both modules have the same number (not positions) of channels activated	Only channel 0 to channel 3 or the both first channels on both modules can be activated
Clock	UF2 card series	UF card series
Available clock modes	PLL, Quartz1, Custom Quartz, External, External reference	PLL, Quartz, External, External reference
Additional clock divider resolution	2 to 8190 in steps of 2	16 fixed divider values
Internal PLL reference clock	10 MHz 20 ppm clock	40 MHz, 50 ppm clock
PLL settings granularity	Improved granularity independent of the number of activated channels and the used mode	limited granularity depending on the number of activated channels and the used mode
External clock ranges	Maximum 2 ranges, lowest range going from DC to 50 MHz / channels per module	Maximum 5 ranges, lowest range going from DC to 5 MHz / channels per module

Trigger	UF2 card series	UF card series
Trigger conjunction	AND and OR conjunction of any trigger source including the mixture of external and channel triggers	OR conjunction of channel triggers
External triggers	1 as standard and 2 additional with option BaseXIO	1 external trigger
Pulse width counter width	16 bit wide	8 bit wide
Delay trigger	0 to 64 kSamples programmable in steps of 1	not available
Enable / disable trigger by command during runtime	available	not available
Option overview	M2i card series	UF card series
Memory upgrades	up to 4 GByte as specified in the memory section	up to 512 MByte as specified in the memory section
Multiple Recording	available as firmware option	available as firmware option
Gated Sampling	available as firmware option	available as firmware option
Timestamp	available as firmware option	available as extension module
ABA mode	available as firmware option	not available
Cascading synchronization	superseded by star-hub 5 option	available as hardware option
Star-Hub 5	available as extension module	not available
Star-Hub 16 (smod)	available as extension module	available as extension module
Later synchronization of already fielded cards	No update needed, all cards are prepared for synchronization, one card need to be equipped with star-hub 5 or star-hub 16	cards need to be sent back to Spectrum and synchronization need to be soldered depending on the mode. If using cascading all cascaded cards have to be synchronized
Extra I/O	BaseXIO option: adds 8 digital I/O lines on the base card. I/O lines can be used for extended trigger and timestamp also	available as extension module offering 24 digital I/O lines and 4 analog outputs
Synchronization option	UF2 card series	UF card series
Available options	star-hub 5 and star-hub 16	cascading and star-hub 16 (smod)
Needed size	star-hub 5: only one slot star-hub 16: two slots	cascading: only one slot smod: two slots
Phase delay	star-hub 5: no phase delay star-hub 16: no phase delay	cascading: ca. 500 ps between adjacent cards smod: no phase delay
Card trigger connection abilities	star-hub 5: AND and OR trigger for all cards and channels star-hub 16: AND and OR trigger for all cards and channels	cascading: one card is trigger source, no trigger connections smod: OR trigger for all cards and channels
Pretrigger area synchronization, enabling of trigger machines from all cards when using different memory sizes or sampling rates	Fully implemented in hardware, all combinations of pretrigger, posttrigger, memory size and clock rates are automatically synchronized through the cards, trigger machine is enabled as soon as all cards are prepared to accept trigger	No hardware synchronization, memory size and sampling clock must match. Start need to be delayed in software to allow different pretrigger areas.
Multiple Recording option	M2i card series	UF card series
Programmable segment size	Minimum 8 samples up to 8 GSample / installed memory in steps of 4 samples	Minimum and stepsize depend on number of activated channels: 64 / channels / bytes per sample. Maximum depends on the number of activated channels: 256 MSamples / channels / bytes per sample
Programmable pretrigger	Up to ((32 kByte - 32) / channels / bytes per sample)	not available
Delay of trigger edge to first sample	no delay as pre- and posttrigger are freely programmable	fixed delay depending on card type, mode, activated channels, activated synchronization and used trigger mode
Programmable delay trigger	from 0 to 64 kSamples in steps of 1	not available
Programmable number of segments in FIFO mode	Available in hardware with 100% defined stop at end of last segment	Programmable in software, counting the number of transferred buffers, some more data is acquired or generated as stop is done by software command
Gated Sampling option	UF2 card series	UF card series
Programmable pretrigger	Up to ((32 kByte - 32) / channels / bytes per sample)	not available
Programmable posttrigger	Fully programmable	not available
Gate stop alignment	Stops are aligned on 4 byte positions (4 sum samples on 8 bit cards, 2 sum samples on 12/14/16 bit cards)	Stops are aligned on 16 byte positions (16 sum samples on 8 bit cards, 8 sum samples on 12/14/16 bit cards)
Delay of trigger edge to first sample	no delay as pre- and posttrigger are freely programmable	fixed delay depending on card type, mode, activated channels, activated synchronization and used trigger mode
Programmable delay trigger	from 0 to 64 kSamples in steps of 1	not available
Programmable number of gate segments in FIFO mode	Available in hardware with 100% defined stop at end of last gate segment	not available

Timestamp option	UF2 card series	UF card series
Shape of option	Firmware option, no additional hardware needed	Extension module
Counter width	56 bit	56 bit
Available timestamp modes	Standard, Start-Reset, RefClock mode	Standard, Start-Reset, Refclock mode
Fed in of RefClock signal	Included in option BaseXIO, no additional slot occupied	As an extra option on demand, additional connector is soldered on the back of the extension module, occupying the neighbour slot
Timestamp memory	4 kByte FIFO with its own DMA engine running in busmaster scatter-gather demand mode. Capable of transferring up to 100 MB/s of sustained data	512 kByte FIFO with PIO access by kernel driver

Software

The comparison of the software features is based on the driver versions that have been available when first writing this application notes. Any changes to the drivers after march 2006 are not mentioned in this comparison list.

Basic Driver Interface	UF2 card series	UF card series
Driver Type	Software register based easy to use driver interface	Software register based easy to use driver interface
Available driver functions	7 functions (+ additional 5 sub-functions)	5 functions
Open/Close	Handle based open and close routines that allow access to different cards from different application programs	One initialization routine that gains exclusive access to all Spectrum cards for one application program
Software register access	SetParam, GetParam with different call types to allow access to 64 bit registers	SetParam, GetParam
Data transfer	Two functions for transfer buffer definition and invalidation	Two functions for read and write data transfer
Error handling	Separate error handling function generating a printable error message	Error handling via software registers
Windows driver	Using standard library interface	Using standard library interface
Linux driver	Using standard library interface, identical to windows driver interface	Using direct kernel driver access with a slightly modified driver interface compared to windows driver interface
Linux driver files	Divided into library and kernel module	One kernel module including kernel and library
Commands	UF2 card series	UF card series
Start command + status polling	available	available
Start command + waiting for ready interrupt	available	available
Waiting for ready interrupt with timeout	available	not available
Waiting for pretrigger ready	available	not available
Waiting for trigger received	available	not available
Poll for trigger received	available	available
Start command + later waiting for ready interrupt	available	not available
Force trigger command	available	available
Enable / disable trigger command	available	not available
Wait for FIFO buffer ready interrupt	available	available
Poll for FIFO buffer ready	available	not available
Wait for FIFO buffer ready interrupt with timeout	available	not available
Software updates	UF2 card series	UF card series
Firmware update	available per integrated software (Spectrum control center)	available using third-party software and special programming cable.
Later feature update	available per integrated software using an update code	available per individually compiled update software
Data transfer	UF2 card series	UF card series
Transfer of data chunks defined by offset and length	available	available
Timeout for data transfer	available	not available
Non-blocking wait for end of data transfer	Yes	No, function returns after complete transfer has finished
Splitted start of transfer and wait for end	Yes	No
FIFO application data buffer organization	One buffer with any size that fits into the memory, notification of new data can be programmed with stepsize of 4k	Up to 256 buffers of the same length like hardware double buffer. Notification of new data is stuck to the buffer length
Polling data transfer status	available	not available
DMA mode of data transfer	Busmaster Scatter-Gather DMA with hardware demand mode (more robust against system background jobs and other tasks)	Busmaster Scatter-Gather DMA handled by the kernel driver
Data transfer for timestamps (and ABA)	Second busmaster Scatter-Gather DMA engine with hardware demand mode	Kernel driver base PIO mode
Start of data transfer in all acquisition single modes	Data transfer can start as soon as first trigger is received and runs while acquisition is still running	Data transfer can earliest start if all data has been recorded