UF.248 : 200 MS/s, 8-Bit resolution, 2 Analog Inputs, PCI

- **High speed PCI interface**
- **2 analog inputs with 8 bit resolution**
- **Simultaneous sampling on both channels**
- **200 MS/s sampling on 2 channels**
- **400 MS/s sampling on 1 channel**
- **Standard memory 32 MSample**
- **Up to 512 MSample Memory**
- **Automatic offset adjust**
- **Input ranges from ±100 mV to ±5 V**
- **SBench 5 software included**
- **Clock and trigger in/output**

Software/Drivers

A large number of drivers and examples are delivered with the board or are available as an option:

- Windows 98/ME/NT/2000/XP - drivers
- Linux - drivers
- SBench 5.2
- Microsoft Visual C++ examples
- Borland Delphi examples
- Microsoft Visual Basic examples
- Microsoft Excel examples
- LabWindows/CVI examples
- FlexPro support with SBench
- LabVIEW - drivers (as option)
- DASYLab - drivers (as option)
- MATLAB - drivers (as option)
- Agilent VEE - drivers (as option)

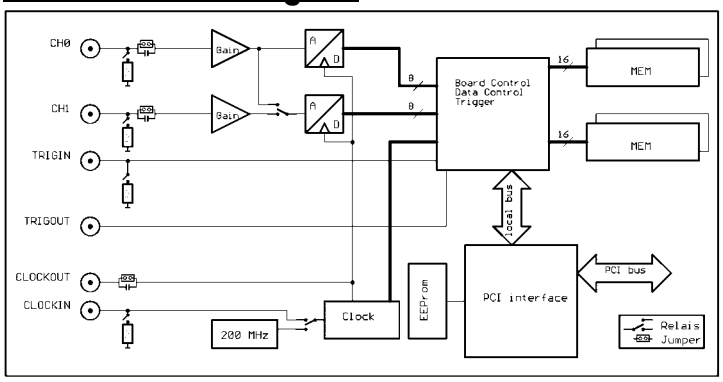
General Information

The UF.248 is a high-quality Transient Recorder and Digitizer board for recording analog signals up to 400 MSamples/s on one channel or 200 MSamples/s on two channels simultaneously. Different modes, e.g. memory segmentation, internal/external clock and trigger as well as the pre- and posttrigger capability makes it easy to adapt this recorder to the measuring problem. The large on-board memory allows the recording of signals with extremely wide bandwidth. Additionally the board has bus master capabilities, so it is able to transfer the measured data directly to the PC's memory.

Application examples

LDA/PDA	Production test
Radar	Spectroscopie
Ultrasound	Medical equipment
Laboratory equipment	Test of mobile communication

Hardware block diagram



Software programmable parameters

sampling rate	2 MS/s to 400 MS/s, external clock
Input range	±100 mV, ±200 mV, ±500 mV, ±1 V, ±2 V, ±5 V
Input Impedance	50 Ohm / 1 MOhm (relais)
Input coupling	AC / DC (jumper)
Clock input	50 Ohm or >24 kOhm
Memory depth	64 Samples up to installed memory in increments of 64 samples
Trigger input	50 Ohm / 1 MOhm (relais)
Triggermode	channel 0, channel 1, external, software
Triggerlevel	1/16 ... 15/16 of the input range
Triggeredge	rising or falling edge
Pulsewidth	0 to 254 samples in increments of 2
Posttrigger	32 Samples up to 256 MSamples in increments of 32 samples

Software Support

Windows drivers

The cards are delivered with drivers for Windows 2000 and Windows XP. Programming examples for Visual C/C++, Borland C++ Builder, LabWindows/CVI, Borland Delphi and Visual Basic are included.

Linux Drivers

All cards are delivered with full Linux support. Pre compiled kernel modules are included for the most common distributions like RedHat, Fedora, Suse or Debian. The Linux support includes SMP systems, 32 bit and 64 bit systems, versatile programming examples for Gnu C++ as well as the possibility to get the driver sources for own compilation.

SBench

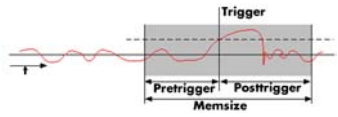
fThe UF2 cards come with a full licence of the SBench program for measurement, analysis and reports. Version 6 is runs under Windows as well as under Linux (KDE and GNOME).

Third-party products

Drivers are available as a cost-option for LabVIEW, MATLAB, DASYLab and Agilent VEE. All drivers come with examples and detailed documentation.

Possibilities and options

Ring buffer mode



The ring buffer mode is the standard mode of all oscilloscope boards. Data is written in a ring memory of the board until a trigger event is detected. After the event the posttrigger values are recorded. This allows the user to record samples prior to the trigger event: Pretrigger = Memsize - Posttrigger.

Input impedance

All inputs could individually be switched by software between 50 Ohm and 1 MOhm input impedance. If using fast signals and high sampling rates or have 50 Ohm cable impedance the use of the 50 Ohm termination is recommended to minimise noise and signal reflections. If using weak signal sources or standard probes the use of the 1 MOhm termination is helpful.

Channel trigger

The data acquisition boards offer a wide variety of trigger modes. In addition to the standard level and edge trigger known from oscilloscopes, it's also possible to define a window trigger. All trigger modes can be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses.

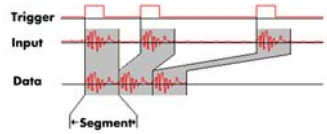
External trigger I/O

All boards can be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulse width. An internally recognised trigger event can - when activated by software - be routed to the trigger connector to start external instruments.

Pulse width

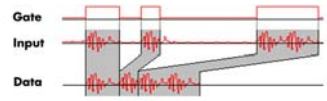
Defines the minimum or maximum width that a trigger pulse must have to generate a trigger event. Pulse width can be combined with channel trigger, pattern trigger and external trigger.

Multiple Recording



The Multiple Recording option allows the recording of several trigger events without restarting the hardware. With this option very fast repetition rates can be achieved. The on-board memory is divided in several segments of same size. Each of them is filled with data if a trigger event occurs.

Gated Sampling



The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level.

External clock I/O

Using a dedicated connector a sampling clock can be fed in from an external system. It's also possible to output the internally used sampling clock to synchronise external equipment to this clock.

Technical Data

Resolution	8 bit	Dimension	312 mm x 107 mm
Samplerate (internal clock)	2 MS/s up to 400 MS/s	Connector	3 mm SMB male
Samplerate (external clock)	25 MS/s up to 200 MS/s	Warm up time	10 minutes
Bandwidth DC -3 dB	0 Hz to ³ 150 MHz	Operating temperature	0°C - 50°C
Bandwidth AC -3 dB	40 Hz to ³ 150 MHz	Storage temperature	-10°C - 70°C
Differential linearity error	< ±1.5 LSB (ADC)	Humidity	10% to 90% non condensing
Integral linearity error	< ±1.5 LSB (ADC)	Overvoltage protection (range ≤ ±1 V)	±5 V
Aperture jitter	2.3 ps rms (ADC)	Overvoltage protection (range > ±1 V)	±50 V
Input impedance	50 Ohm / 1 MOhm || 25 pF	ext. Trigger accuracy (<200 MS/s)	2 Samples
Multi: Trigger to 1st sample delay	19 to 44 (fix)	ext. Trigger accuracy (400 MS/s)	4 Samples
Multi: Recovery time	< 20 samples	int. Trigger accuracy	1 Sample
ext. clock input	ECL, AC coupled	Power consumption at +5 V	2.5 A (12.5 W)
Ext. clock: delay to internal clock	< 3 ns	Power consumption at ±12 V	0.01 A (0.12 W) / 0.1 A (1.2 W)

Dynamic Parameters

	1 MHz test signal	4.5 MHz test signal
Sample rate	200 MS/s	200 MS/s
Test input range	± 500 mV	± 500 mV
SNR (typ)	> 40.0 dB	> 39.5 dB
THD (typ)	> 52,2 dB	> 51.0 dB
SFDR (typ), incl harm.	> 47.0 dB	> 47.0 dB
SINAD (typ)	> 39.5 dB	> 39.5 dB
ENOB (based on SINAD)	> 6.3	> 6.3

Dynamic parameters are measured at ± 1 V input range (if no other range is stated) and 50 Ohm termination with the samplerate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits. For a detailed description please see application note 002.

Order information

Order No	Description	Order No	Description
UF.248	UF.248 with 32 MSample memory and drivers/SBench 5.x	UF.200-64	Option: 64 MSample memory instead of 32 MSample standard mem
UF.200-mr	Option Multiple Recording: Memory segmentation	UF.200-256	Option: 256 MSample mem instead of 32 MSample standard mem
UF.200-gs	Option Gated Sampling: Gate signal controls acquisition	UF.200-512	Option: 512 MSample mem instead of 32 MSample standard mem
UF.200-dm	Double Mem: Channel 0 uses complete memory at every samplerate	UF.200-up	Additional handling cost for later memory upgrade
Cab-3f-9m-80	Adapter cable: SMB female to BNC male 80 cm	UF.200-dl	DASYLab driver for UF.248 series
Cab-3f-9m-200	Adapter cable: SMB female to BNC male 200 cm	UF.200-hp	VEE driver for UF.248 series
Cab-3f-9f-80	Adapter cable: SMB female to BNC female 80 cm	UF.200-lv	LabVIEW driver for UF.248 series
Cab-3f-9f-200	Adapter cable: SMB female to BNC female 200 cm	UF/UC/UX-ml	MATLAB driver for all PCI boards.

technical changes and printing errors possible

STRATEGIC TEST
The High-Speed Specialists

STRATEGIC TEST CORPORATION · STOCKHOLM, SWEDEN · WOBURN, MA, USA
EUROPE PHONE: +46 (854)400-490 · USA PHONE: +1 (617)621-0080 · E-MAIL: info@strategic-test.com · INTERNET: http://www.strategic-test.com