



UX.4700 : 8 channel 16 bit A/D Digitizers / Oscilloscopes, up to 500 kS/s

- **PXI 3U / CompactPCI 3U format**
- **8 channels with 16 bit resolution per card**
- **Versions with 100 kS/s up to 500 kS/s**
- **Simultaneous sampling on all channels**
- **Separate ADC and amplifier per channel**
- **Complete on-board calibration**
- **8 input ranges: ± 50 mV up to ± 10 V**
- **Up to 64 MSample (128 MByte) on-board memory**
- **Sustained streaming mode up to 100 MB/s**
- **Window, pulse width, re-arm, spike trigger**
- **OR/AND trigger combinations possible**
- **Synchronization possible**



Product range overview

The UltraFast PXI cards are based on more than 16 years design experience. The cards are high-quality, low-noise PC-based instruments that have deeper memory and more flexibility than traditional oscilloscopes and transient recorders.

Model	1 channel	2 channel	4 channel	8 channel
UX.4710	100 kS/s	100 kS/s	100 kS/s	100 kS/s
UX.4720	250 kS/s	250 kS/s	250 kS/s	250 kS/s
UX.4730	500 kS/s	500 kS/s	500 kS/s	500 kS/s

Software/Drivers

A large number of drivers and examples are delivered with the board or are available as an option:

- Windows 98/ME/NT/2000/XP - drivers
- Linux - drivers
- SBench 5.2
- Streaming Software SPviewIT 6.2 (as option)
- Visual C++/Borland C++ Builder examples
- Borland Delphi examples
- Microsoft Visual Basic examples
- Microsoft Excel examples
- LabWindows/CVI examples
- FlexPro support with SBench
- LabVIEW - drivers (as option)
- DASyLab - drivers (as option)
- MATLAB - drivers (as option)
- Agilent VEE - drivers (as option)

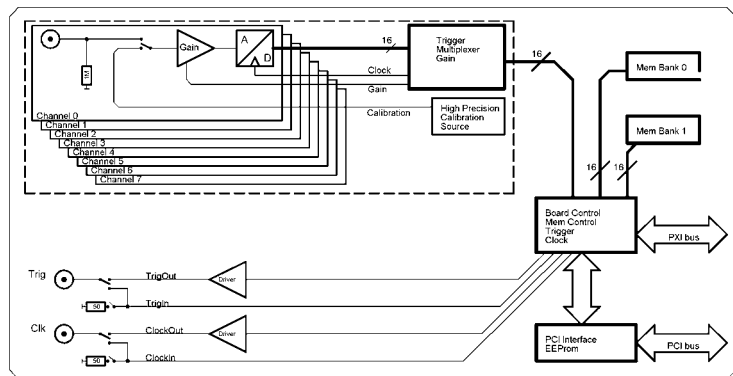
General Information

The UX.4700 for the first time offers full 16 bit resolution on eight synchronous channels at high sampling rates.

Each channel has its own A/D converter so there is no phase error between channels. The voltage range, signal offset and input impedance can be programmed for each channel to match a wide variety of signal sources.

Data is written in the internal 8 MSamples up to 64 MSample large memory. This memory can also be used as a FIFO buffer so that data can be transferred on-line directly into the PC RAM or to hard disk

Hardware block diagram



Software programmable parameters

Sampling rate	1 kS/s to max sampling rate, external clock, ref clock, PXI clock
Input range	± 50 mV, ± 100 mV, ± 250 mV, ± 500 mV, ± 1 V, ± 2 V, ± 5 V, ± 10 V
Clock mode	internal PLL, internal quartz, external, external divided, external reference clock, PXI reference clock
Clock impedance	50 Ohm / 1 MOhm
Trigger impedance	50 Ohm / 1 MOhm
Trigger mode	Channel, External, Software, Auto, Window, Pulse, Spike, PXI Line[5..0], PXI Startrigger
Trigger level resolution	14 bit
Trigger edge	rising edge, falling edge or both edges
Trigger pulsewidth	1 to 255 samples in steps of 1 sample
Memory depth	32 up to installed memory in steps of 32
Posttrigger	32 up to 128 M in steps of 32
Multiple Recording segmentsize	32 up to installed memory / 2 in steps of 32

Possibilities and options

PXI bus

The PXI bus (PCI eXtension for instrumentation) offers a variety of additional standard possibilities for synchronising different components in one system. It is possible to connect several Strategic Test cards with each other or to connect a Strategic Test card with cards of other manufacturers.

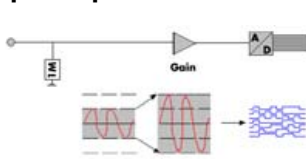
PXI reference clock

The card is able to use the 10 MHz reference clock that is supplied by the PXI system. Enabled by software the PXI reference clock is fed into the on-board PLL. This feature allows the cards to run with a fixed phase relation.

PXI trigger

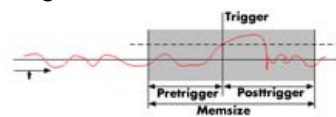
The UX cards support star trigger as well as the PXI trigger bus. Using a simple software command one or more trigger lines can be used as trigger source. This feature allows easy setup of OR connected triggers from different cards.

Input Amplifier



The analog inputs can easily be adapted to real world signals using settings that are individual for each channel. By using software commands one can select a matching input range.

Ring buffer mode



The ring buffer mode is the standard mode for all oscilloscope boards. Data is written in a ring memory of the board until a trigger event is detected. After the event the posttrigger values are recorded. This allows the user to record events both before and after the trigger: $\text{Pretrigger} = \text{Memsize} - \text{Posttrigger}$.

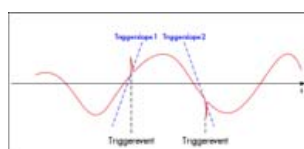
FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 100 MB /s) or hard disk (up to 50 MB/s). The control of the data stream is done automatically by the driver on interrupt request.

Channel trigger

The data acquisition boards offer a wide variety of trigger modes. Besides the standard level and edge triggers known from oscilloscopes, it's also possible to define a window trigger. All trigger modes can be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses.

Spike trigger



When using the spike trigger mode, the difference between two samples is checked whether being higher than the programmed limit or not. This can be useful to trigger e.g. on noise

coming from a power supply.

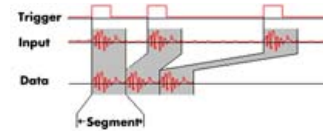
External trigger I/O

All boards can be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulse width. A software trigger event can, when activated by software, be routed to the trigger connector to start external instruments.

Pulse width

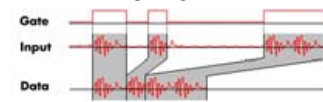
Defines the minimum or maximum width that a trigger pulse must have to generate a trigger event. Pulse width can be combined with channel trigger, pattern trigger and external trigger.

Multiple Recording



The Multiple Recording option allows the recording of several trigger events without restarting the hardware. This enables very fast repetition rates to be achieved. The on-board memory is divided in several segments of same size. Each of them is filled with data if a trigger event occurs.

Gated Sampling

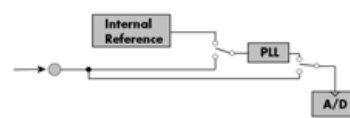


The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level.

External clock I/O

Using a dedicated connector a sampling clock can be fed in from an external system. It's also possible to output the internal sampling clock to synchronise external equipment to this clock.

Reference clock



The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronise the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

Technical Data

Analog Inputs

Resolution	16 bit
Differential non linearity (DNL)	TBD
Integral non linearity (INL)	TBD
Offset error (full speed)	TBD
Gain error (full speed)	TBD
Fixed input mode	bipolar
Crosstalk: all ranges 100 kHz signal	TBD
Analog Input impedance	1 MOhm against GND
Over voltage protection	±30 V all ranges (activated card)
Aliasing filter	Butterworth filter 2nd order

Connector (analog)	MMCX female
Connector (trigger/clock)	3 mm SMB male

Power consumption (max speed)	3,3 V	5 V	-12 V	+12 V	Total
UX.47x0 (8 MS memory)	TBD	TBD	TBD	TBD	TBD
UX.4731 (64 MS memory), max power	TBD	TBD	TBD	TBD	TBD

Trigger input: Standard TTL level	Low: -0.5 V > level < 0.8 V High: 2.0 V > level < 5.5 V Trigger pulse must be valid ≥ 2 clock periods.
Trigger output	Standard TTL, capable of driving 50 Ohm. Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA) One positive edge after the first internal trigger

Ext. clock: delay to internal clock 42 ns ± 2 ns

Trigger

Multi: Trigger to 1st sample delay	fixed
Multi: Recovery time	< 20 samples
ext. Trigger accuracy	1 Sample
int. Trigger accuracy	1 Sample
input signal with 50 ohm termination	max 5 V rms
Trigger output delay	1 Sample

Environmental and Physical details

Dimension	160 mm x 100 mm (Standard 3U)
Width (standard board)	1 slot
Warm up time	10 minutes
Operating temperature	0°C - 50°C
Storage temperature	-10°C - 70°C
Humidity	10% to 90%

Certifications and Compliances

EMC Immunity	Compliant with CE Mark
EMC Emission	Compliant with CE Mark

Clock input: Standard TTL level	Low: -0.5 V > level < 0.8 V High: 2.0 V > level < 5.5 V Rising edge. Duty cycle: 50% ± 5%
Clock output	Standard TTL, capable of driving 50 Ohm Low < 0.4 V (@ 20 mA, max 64 mA) High > 2.4 V (@ -20 mA, max -48 mA)

	UX.4710	UX.4720	UX.4730
Min internal clock	1 kS/s	1 kS/s	1 kS/s
Max internal clock	100 kS/s	250 kS/s	500 kS/s
Min external clock	TBD	TBD	TBD
Max external clock	100 kS/s	250 kS/s	500 kS/s
-3 dB bandwidth	TBD	TBD	TBD

Dynamic Parameters

	UX.4710	UX.4720	UX.4730
Test - sampling rate	100 kS/s	250 kS/s	500 kS/s
Test signal frequency	TBD	TBD	TBD
SNR (typ)	TBD	TBD	TBD
THD (typ)	TBD	TBD	TBD
SFDR (typ), incl harm.	TBD	TBD	TBD
SINAD (typ)	TBD	TBD	TBD
ENOB (based on SINAD)	TBD	TBD	TBD

Dynamic parameters are measured at ±5 V input range (if no other range is stated) and 1 MOhm termination with the sampling rate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits. For a detailed description please see application note 002.

Order Information

Versions	Order no.	1 channel	2 channels	4 channels	8 channels
	UX.4710	100 kS/s	100 kS/s	100 kS/s	100 kS/s
	UX.4720	250 kS/s	250 kS/s	250 kS/s	250 kS/s
	UX.4730	500 kS/s	500 kS/s	500 kS/s	500 kS/s

Options	Order no.	Option
	UX.4700-mr	Option Multiple Recording
	UX.4700-gs	Option Gated Sampling

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	UX.4700-mr	Option Multiple Recording
	UX.4700-gs	Option Gated Sampling

Cables	Order no.	Option
	Cab-1m-9m-80	Adapter cable MMCX male to BNC male, 80 cm (for analog inputs)
	Cab-1m-9f-80	Adapter cable MMCX male to BNC female, 80 cm (for analog inputs)
	Cab-1m-9m-200	Adapter cable MMCX male to BNC male, 200 cm (for analog inputs)
	Cab-1m-9f-200	Adapter cable MMCX male to BNC female, 200 cm (for analog inputs)
	Cab-1m-9f-5	Adapter cable MMCX male to BNC female, 5 cm (short cable especially for oscilloscope probes)
	Cab-3f-9m-80	Adapter cable SMB female to BNC male, 80 cm (for clock and trigger I/O)
	Cab-3f-9f-80	Adapter cable SMB female to BNC female, 80 cm (for clock and trigger I/O)
	Cab-3f-3f-80	Adapter cable SMB female to SMB female, 80 cm (for clock and trigger I/O)
	Cab-3f-9m-200	Adapter cable SMB female to BNC male, 200 cm (for clock and trigger I/O)
	Cab-3f-9f-200	Adapter cable SMB female to BNC female, 200 cm (for clock and trigger I/O)
	Cab-3f-3f-200	Adapter cable SMB female to SMB female, 200 cm (for clock and trigger I/O)

Drivers	Order no.	Option
	UF/UC/UX-ml	MATLAB driver for all UF/UC/UX cards
	UX.4700-lv	LabVIEW driver for all UX.4700 cards
	UX.4700-dl	DASyLab driver for all UX.4700 cards
	UX.4700-vee	Agilent VEE driver for all UX.4700 cards

technical changes and printing errors possible

